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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,960	07/15/2003	Giora Biran	IL920000076US1	7798

54856 7590 02/21/2007	EXAMINER	
LOUIS PAUL HERZBERG	PARK, ILWOO	
3 CLOVERDALE LANE		
MONSEY, NY 10952	ART UNIT	PAPER NUMBER
	2182	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	10/619,960	BIRAN ET AL.
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claim 21 is added in response to the last office action. Claims 1-21 are

presented for examination.

Response to Arguments

2.   Applicant's arguments filed 11/20/2006 have been fully considered but they are

not persuasive. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they

amount to a general allegation that the claims define a patentable invention without

specifically pointing out how the language of the claims patentably distinguishes them

from the references.

In the Remarks, Applicant argues in substance that the cited art to Osborne has

little or no relevant to claim 1 because a) Osborne does not teach the descriptor table;

ring queue 16 of Osborne is a transmit input queue and not a descriptor table for storing

a plurality of descriptors for access by the first and second data processing system; b)

Osborne is not relevant to flow control between data processing systems; c) Osborne

does not teach generating the descriptors for storage in the descriptor table.

The Examiner respectfully disagrees with the Applicant's arguments. Applicant is

required to see the cited reference as a whole.

The host and the network interface <u>commonly use</u> ring queues for communication of data
and synchronization between the host and network interface. A ring queue, or circular queue, is
a common data structure in which a first-in first-out or FIFO queue wraps around, such that the
queue occupies a fixed size and extent of memory. [Osborne: col. 1, lines 59-64]
Typically, two of these <u>ring queues</u> are allocated for the transmit side and two to the
<u>receive side within the network interface.</u> With respect to the transmit side, one of the queues in
the transmit side indicates frames to be transmitted. <u>Each entry in this "transmit input" queue</u>
describes a frame. Hence <u>the entries are known as frame descriptors</u>. The second queue on the
transmit side is a "transmit complete" queue which <u>contains descriptors</u> of frames that have
been transmitted. On the receive side, one queue is a "free buffer" queue <u>containing descriptors</u>

describing empty buffers. A second queue on the receive side is typically a "receive complete" queue in which the entries are frame descriptors which describe the frame data which has been received.   [Osborne: col. 1, line 59-col. 2, line 10]

In operation, the host inserts a frame descriptor at the tail of the transmit input queue and notifies the network interface that there is a frame descriptor to be acted upon. There are, of course, many ways to notify the network interface that there is a frame descriptor to be processed. One way is for the network interface to respond to host updates to the tail pointer by reading the entry at the head position.   [Osborne: col. 2, lines 15-21]

Referring now to FIG. 2B, the Fujitsu interface has an input queue 80 in which each entry such as 82 is a single pointer to a transmit buffer descriptor such as 84 in a buffer descriptor table 86.   [Osborne: col. 13, lines 20-23]

Buffer descriptor 84 has an entry 92 which is a pointer to a buffer 94. The transmit buffer descriptors are chained within the table as illustrated at 96 and 98. In operation, when the network interface finds an entry in input queue 80, it examines the buffer descriptor to determine on which virtual channel the buffer is to be sent. It then indexes into a circuit table to determine on which of 12 fixed rate queues the frame should be enqueued for transmission. These 12 queues are shown by references 98A-98L.   [Osborne: col. 13, lines 24-32]

For the point a), as seen above, Osborne teaches the descriptor table [ring queue, such as transmit input queue, free buffer queue, etc.] storing a plurality of descriptors [containing frame descriptors and/or buffer descriptors] for access both by the first data processing system [host in fig. 3A] and by the second data processing system [network interface card in fig. 3A].

Referring to FIG. 3A, in the subject invention the flexible format of frame descriptors and buffer descriptors permit the aforementioned functions and advantages. To illustrate how this is possible in general, an ATM network interface includes a network interface card 150 and a host computer 151. The frame descriptors and buffer descriptors are used for communication between host 151 and network interface card 150 over peripheral component interconnect or PCI bus 152. The communication includes control information for the ring queues and information describing the data to be transmitted or describing data received. This information belongs to the network interface. Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory.   [Osborne: col. 14, lines 21-35]

For the point b), fig. 3A and its relevant description of Osborne describes flow control between data processing systems [host and network interface card] using the plurality of descriptors.

In operation, the host <u>inserts a frame descriptor</u> at the tail of the transmit input queue and notifies the network interface that there is a frame descriptor to be acted upon.   [Osborne: col. 2, lines 15-17]

Specifically, the RX and TX blocks are composed of circuitry designed specifically to interpret the control information format. In this sense, <u>the frame descriptor format and the buffer descriptor format are embodied</u> in these blocks. As such in one embodiment the subject invention is an RX circuit and a TX circuit configured to <u>implement these formats</u>.   [Osborne: col. 15, lines 1-7]

FIG. 9 shows the situation just after the driver/application has <u>enqueued such a frame descriptor</u> in the TXin queue 160.   [Osborne: col. 19, lines 46-47]

For the point c), as seen above, Osborne teaches generating and storing descriptors [inserting into the queue using formats shown in figs. 3B-14].

Therefore, the arguments are not persuasive and rejections are respectfully maintained.

Double Patenting

3.   Claims 1-20 of this application conflict with claims 1-20 of Application No. 10/619,988. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by

Osborne et al. [US 5,751,951].

As for claim 1, Osborne et al teach an apparatus comprising: a descriptor table

[e.g., "ring queue" in col. 1, line 59- col. 2, line 10; col. 5, lines 53-64; col. 14, lines 21-

35], said apparatus for controlling [col. 14, lines 20-35] flow of data between first [host in

fig. 3A and relevant description] and second data processing systems [network interface

card in fig. 3A and relevant description] via a memory, said descriptor table for storing a

plurality of descriptors for access [col. 1, lines 59-64; col. 2, lines 15-21; col. 16, lines 6-

24] by the first and second data processing systems; and descriptor logic for generating

[inserting into the queue using formats shown in figs. 3B-14 and relevant description;

col. 2, lines 15-17; col. 15, lines 1-7; col. 19, lines 46-47] the descriptors for storage in

the descriptor table, the descriptors including a branch descriptor comprising a link [e.g.,

fig. 2A, 2B and relevant description] to another descriptor in the table.

6.   As for claim 2, Osborne et al teach the descriptors generated by the descriptor

logic comprising a frame descriptor defining a data packet to be communicated between

a location in the memory and the second data processing system, and a pointer

descriptor identifying the location in the memory [e.g., figs. 2A-14 and relevant

description; col. 5, lines 53-64].

7.   As for claim 3, Osborne et al teach the descriptor table is stored in the memory of

the first data processing system [host memory in col. 14, lines 32-35].

8.   As for claim 4, Osborne et al teach the descriptor table is stored in the memory of

the second data processing system [local memory of network interface card in col. 14,

lines 32-35; col. 14, lines 57-58].

9.   As for claim 5, Osborne et al teach the descriptor table comprising a plurality of

descriptors lists sequentially linked together via branch descriptors therein [e.g., figs.

2A-2C and relevant description].

10.   As for claim 6, Osborne et al teach the descriptor table comprising a cyclic

descriptor list [col. 1, lines 61-64].

11.   As for claim 7, Osborne et al teach the first data processing system comprising a

host computer system [host in fig. 3A and relevant description].

12.   As for claim 8, Osborne et al teach the second data processing system

comprising a data communications interface for communicating data between a host

computer system and a data communications network [host and network interface card

in fig. 3A and relevant description].

13.   As for claim 9, Osborne et al teach a host computer system having a memory, a

data communications interface for communicating data between the host computer

system and a data communications network for controlling flow of data between the

memory of the host computer system and the data communications interface [fig. 3A

and relevant description].

14.   As for claim 10, Osborne et al teach a method comprising controlling flow of data

between first and second data processing systems via a memory, the steps of

controlling comprising: storing [e.g., figs. 2A-2C and relevant description] in a descriptor

table a plurality of descriptors for access [col. 3, lines 28-42] by the first and second

data processing systems; and by descriptor logic, generating [e.g., col. 19, lines 46-47]

the descriptors for storage in the descriptor table, the descriptors including a branch

descriptor comprising a link [e.g., fig. 2A and relevant description] to another descriptor

in the table.

15.   As for claims 11-21, Osborne et al teach the claimed limitations as discussed

above.

Conclusion

16.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

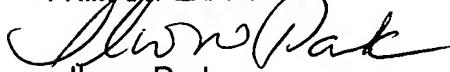than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155.

The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30

PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for

the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park

February 15, 2007